a gate electrode formed above said gate insulation layer, said gate electrode having a middle portion located over the active region, said middle portion having a gate length and a gate height, wherein a cross-sectional area of said gate electrode in a plane defined by said gate length and said gate height of the middle portion exceeds a value obtained by multiplying the gate length by the gate height.

Please add the following new claims 27-34:

SUB B2 A2

27. (New) A transistor, comprising:

a substrate;

a gate insulation layer formed above said substrate; and

a gate electrode formed above said gate insulation layer, said gate electrode having an upper portion and a lower portion, said upper portion having a plurality of extensions formed thereon, said extensions of said upper portion extending laterally beyond said lower portion of said gate electrode.

28. (New) The transistor of claim 27, further comprising an insulating material positioned adjacent said lower portion of said gate electrode and under said extensions formed on said upper portion.

29. (New) The transistor of claim 27, wherein said substrate is comprised of silicon.

30. (New) The transistor of claim 27, wherein said gate insulation layer is comprised f silicon dioxide.